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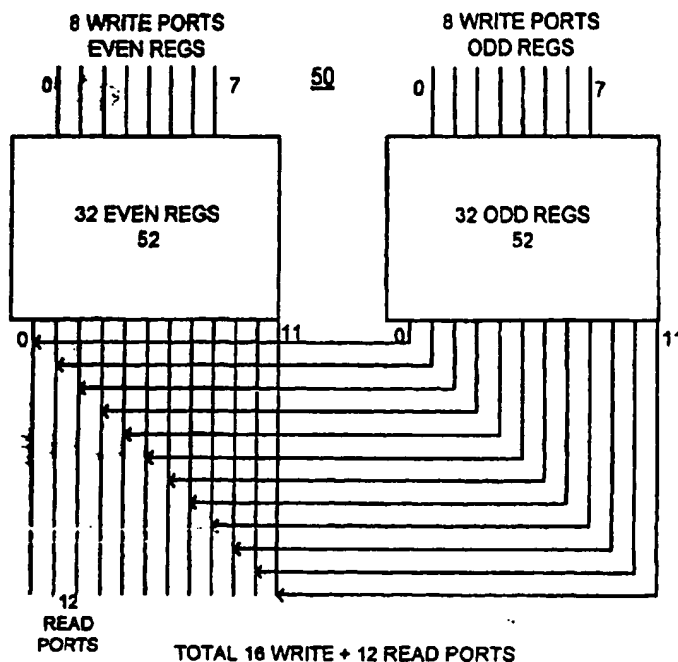
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**(54) Multiple port register file with interleaved write ports**

(57) A high speed register file is provided for use with Very Long Word Instruction (VLIW) and N-way superscaler processors. The high speed register file includes a selected number of copies of a general purpose register (GPR) building block. The GPR building block

includes at least two interleaved sub-banks of registers. Each of the sub-banks includes a number N of write ports and a number M of read ports. The sub-banks are interleaved by write ports and have non-interleaved read ports.



**FIG.1**

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# EUROPEAN SEARCH REPORT

Application Number  
EP 96 48 0056

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (InCL.8)
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A	US 5 392 411 A (OZAKI SHINJI) 21 February 1995 (1995-02-21) * column 4, line 53 - column 7, line 46; figures 2,3 *	1,2,5,7	
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			TECHNICAL FIELDS SEARCHED (Int.Cl.8)
			G06F
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>30 November 2000</b>	Examiner <b>Daskalakis, T</b>
CATEGORY OF CITED DOCUMENTS		T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date O: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document	
X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT  
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82